FOREIGN SEARCHED

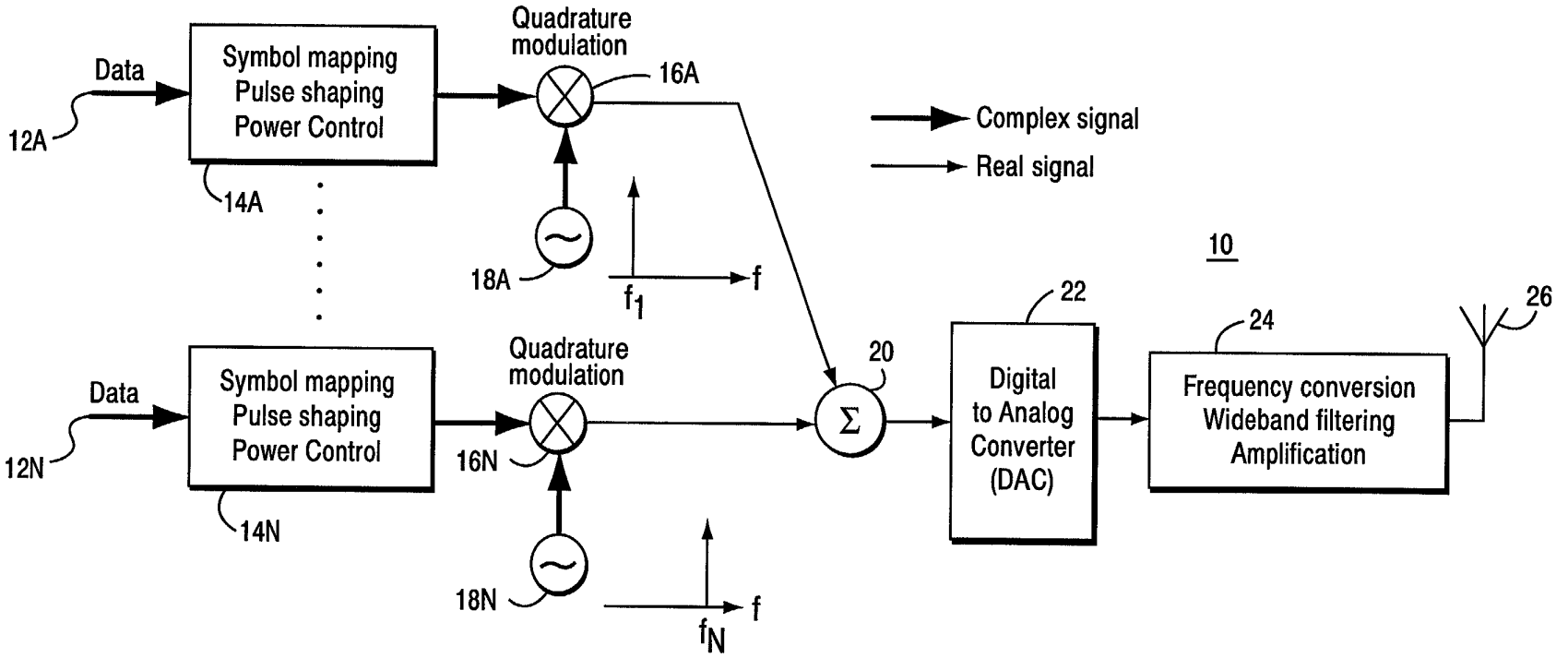

Fig. 1

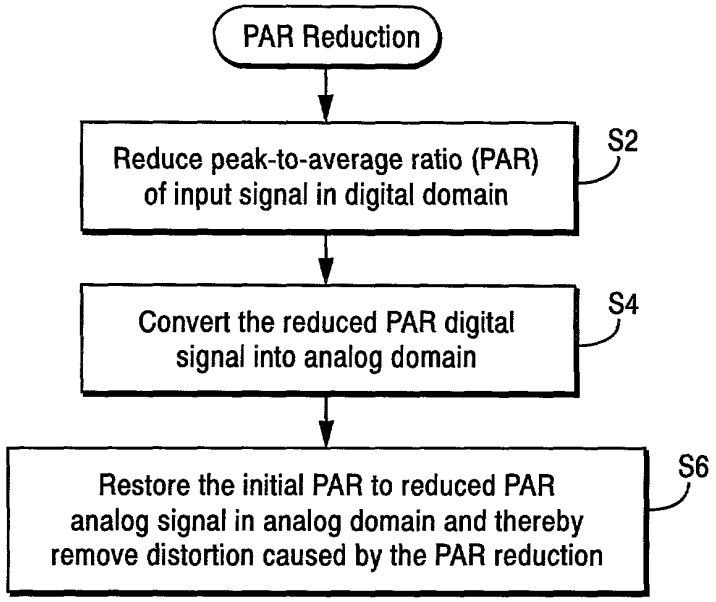
PAR Reduction
Reduce peak-to-average ratio (PAR) of input signal in digital domain
S2
Convert the reduced PAR digital signal into analog domain
S4
Restore the initial PAR to reduced PAR analog signal in analog domain and thereby remove distortion caused by the PAR reduction
S6

Fig. 2

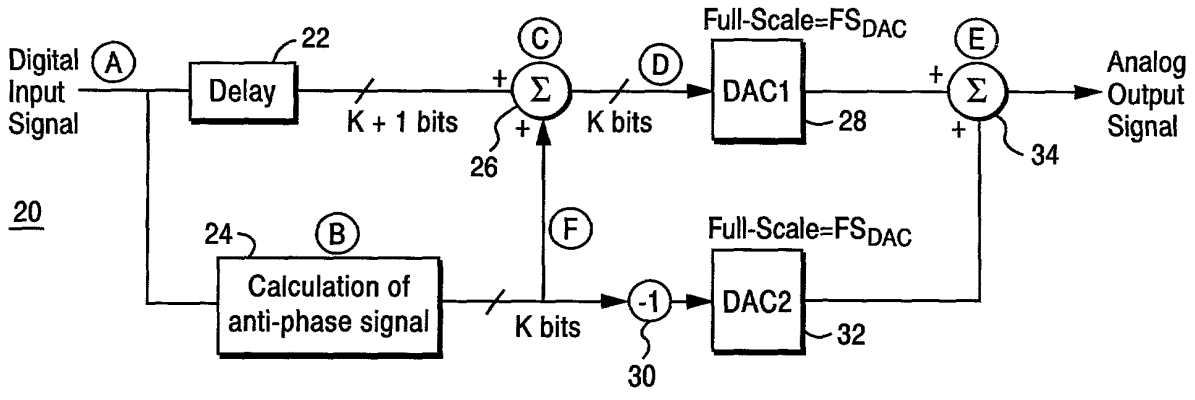
Digital Input Signal
A
Delay
22
K + 1 bits
C
Σ
+
+
26
D
K bits
Full-Scale=FS_DAC
DAC1
28
E
Σ
+
+
34
Analog Output Signal
20
24
B
Calculation of anti-phase signal
F
K bits
-1
30
Full-Scale=FS_DAC
DAC2
32

Fig. 3

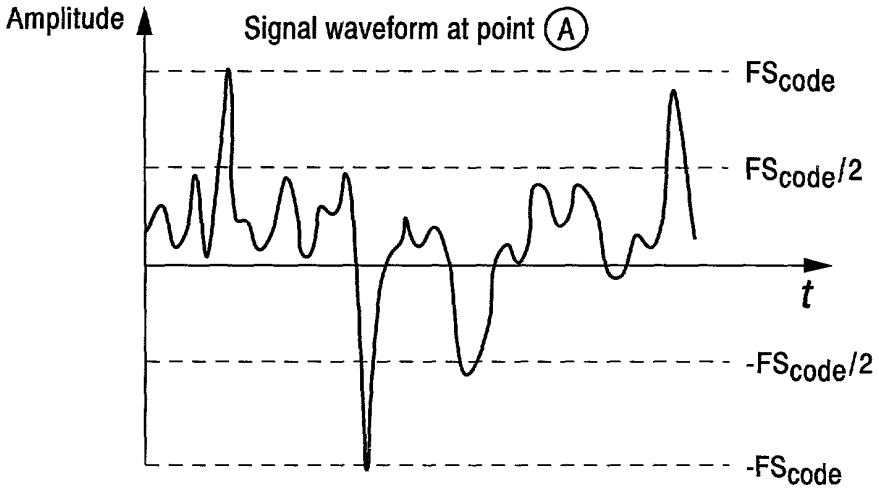

Fig. 4A

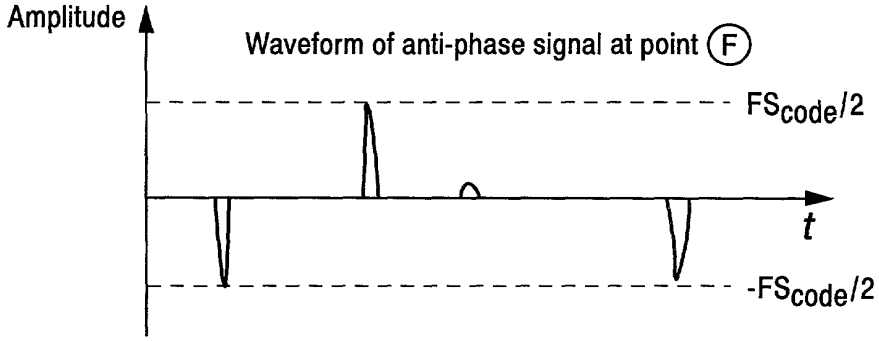

Fig. 4B

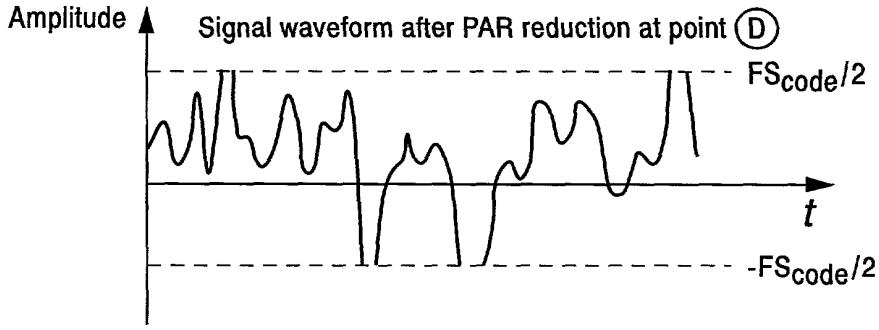

Fig. 4C

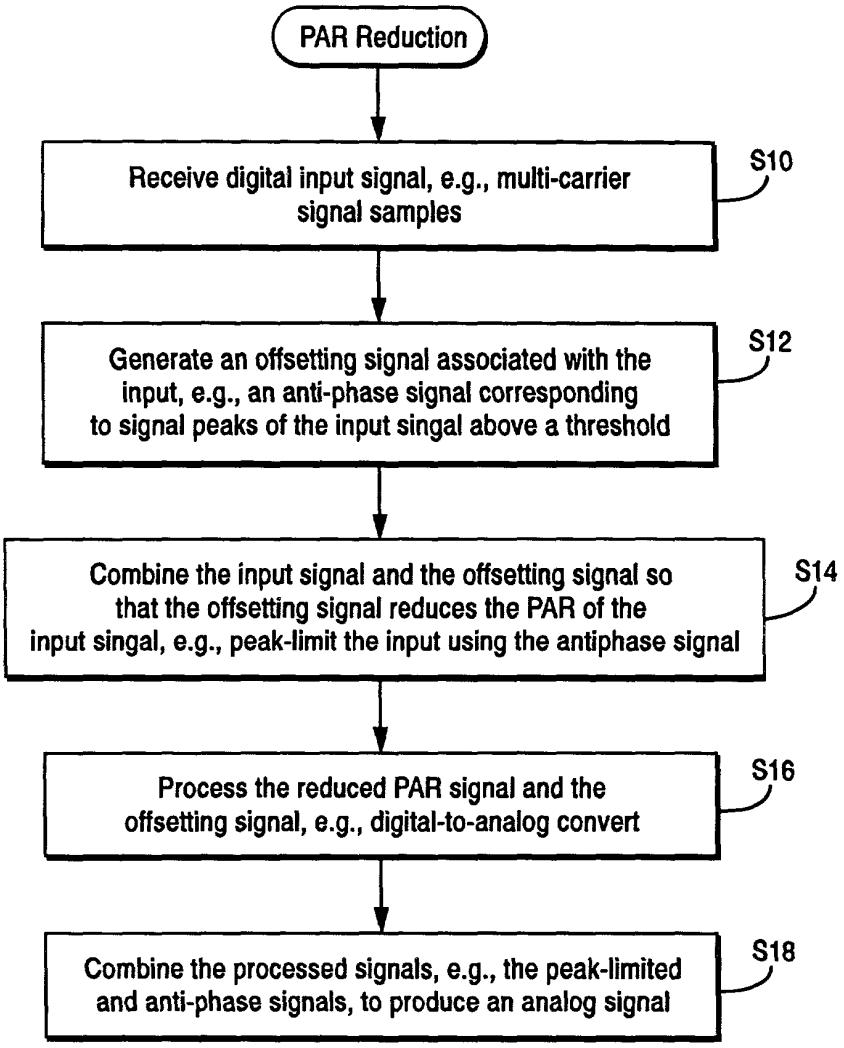
PAR Reduction
Receive digital input signal, e.g., multi-carrier signal samples
S10
Generate an offsetting signal associated with the input, e.g., an anti-phase signal corresponding to signal peaks of the input singal above a threshold
S12
Combine the input signal and the offsetting signal so that the offsetting signal reduces the PAR of the input singal, e.g., peak-limit the input using the antiphase signal
S14
Process the reduced PAR signal and the offsetting signal, e.g., digital-to-analog convert
S16
Combine the processed signals, e.g., the peak-limited and anti-phase signals, to produce an analog signal
S18

Fig. 5

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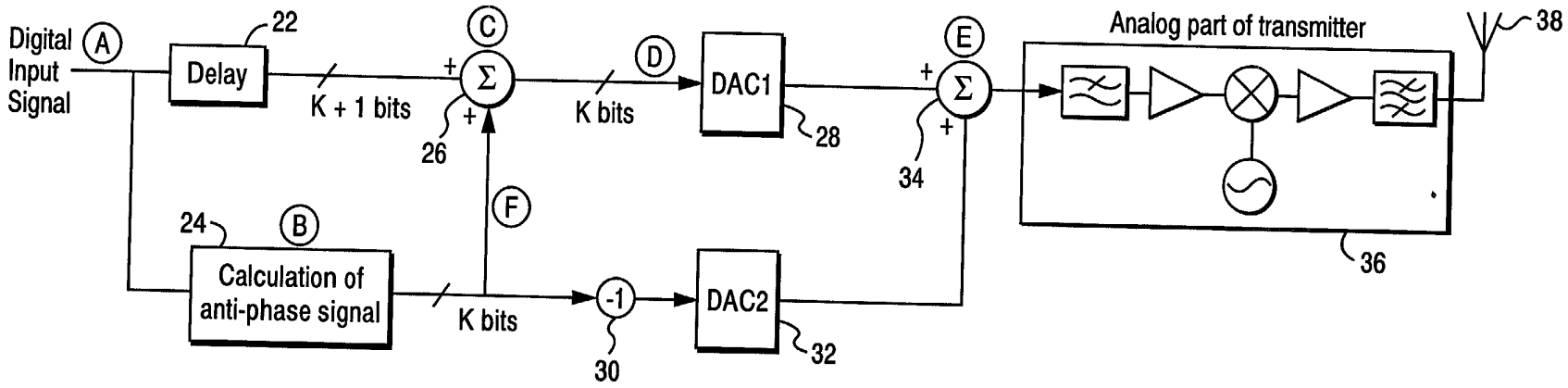

Fig. 6

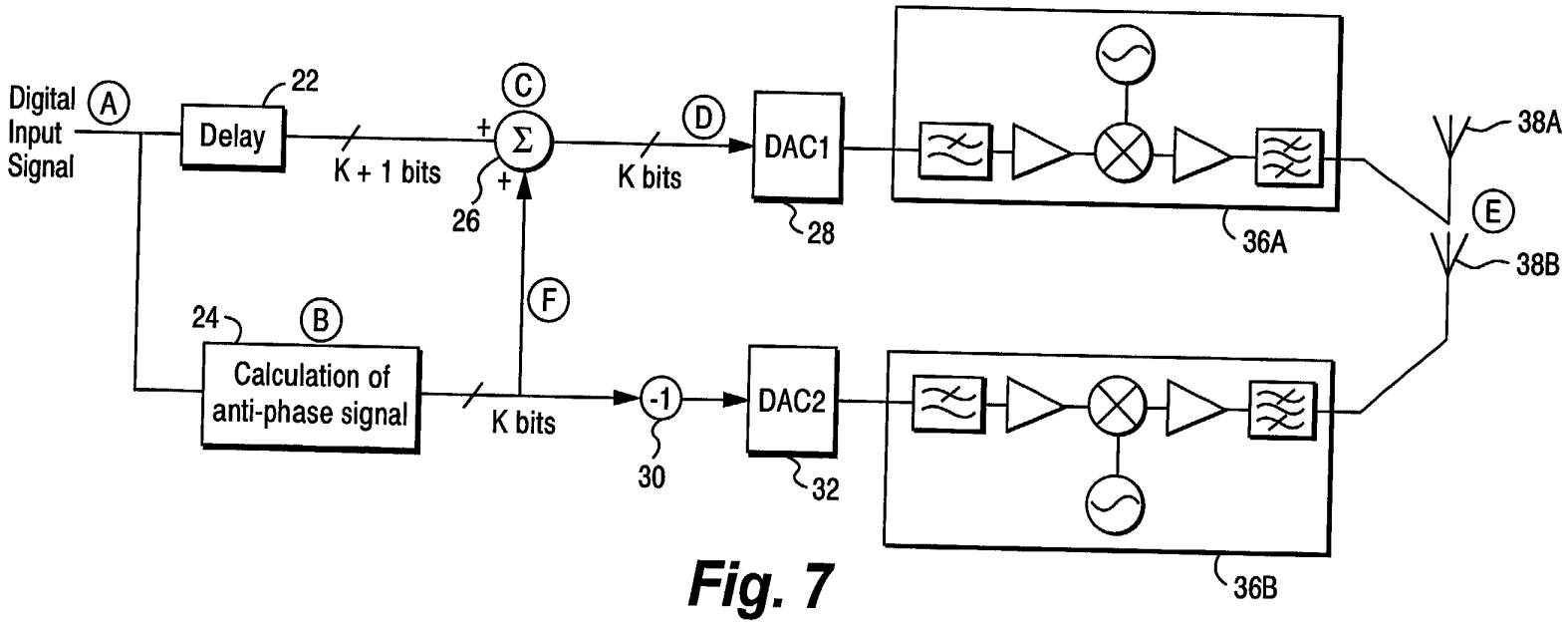

Fig. 7

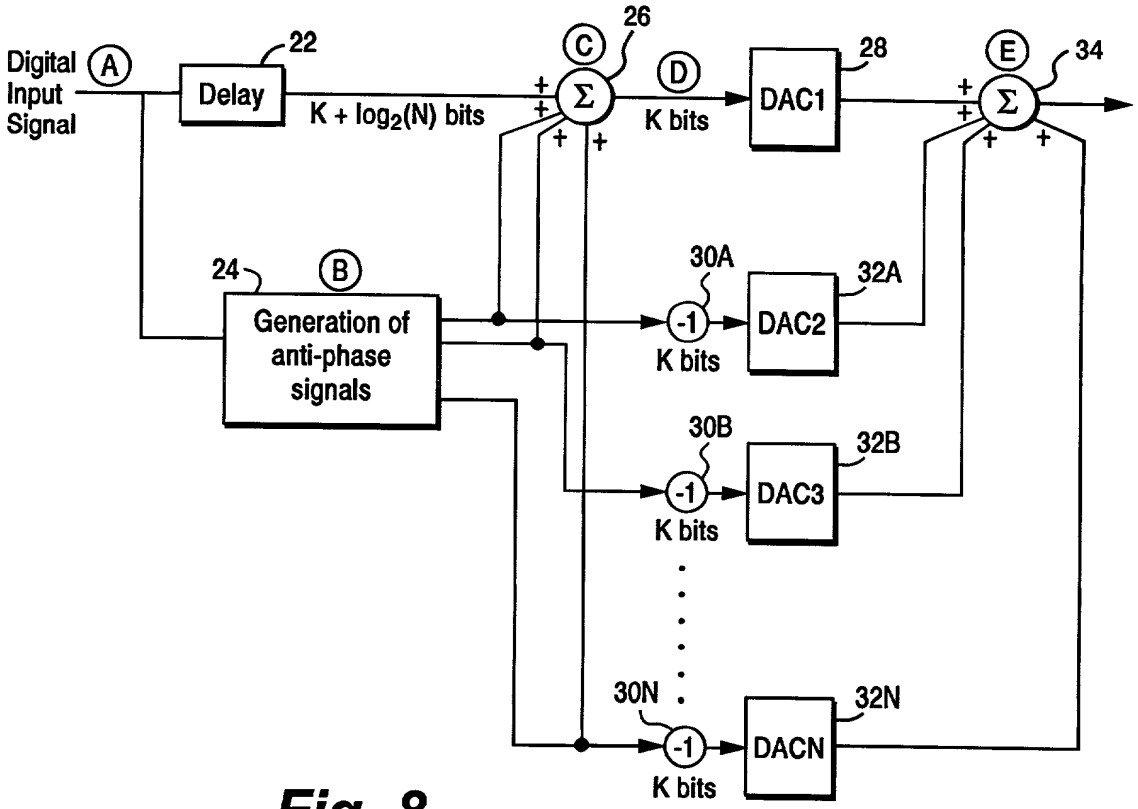
Digital Input Signal
A
Delay
22
K + log2(N) bits
C
26
D
K bits
DAC1
28
E
34
24
B
Generation of anti-phase signals
30A
-1
K bits
DAC2
32A
30B
-1
K bits
DAC3
32B
30N
-1
K bits
DACN
32N

Fig. 8

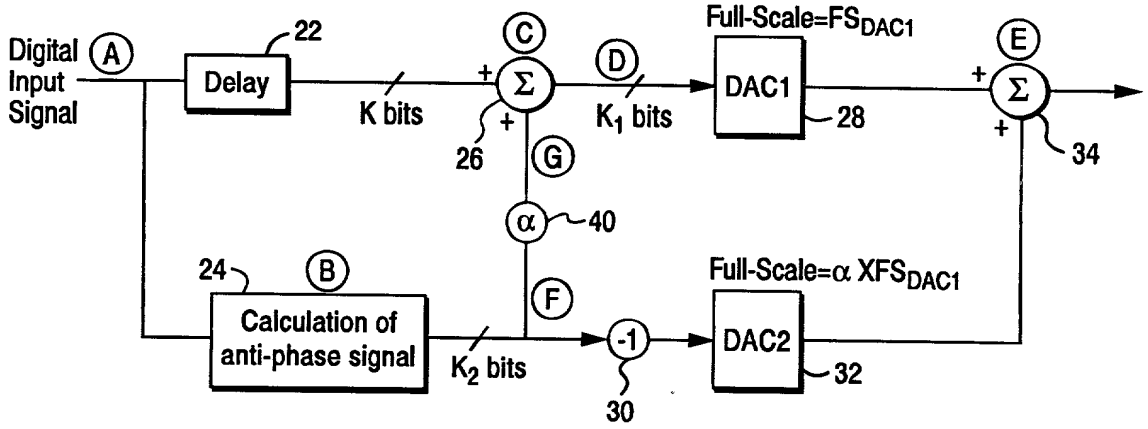
Digital Input Signal
A
Delay
22
K bits
C
26
D
K1 bits
Full-Scale=FSDAC1
DAC1
28
E
34
G
α
40
24
B
Calculation of anti-phase signal
K2 bits
F
-1
30
Full-Scale=α XFSDAC1
DAC2
32

Fig. 9